In the Claims

Claims 1-46 (canceled).

47. (previously presented) An integrated circuit comprising:

integrated circuit wiring over a semiconductive substrate;

an insulation layer enclosing the wiring and a bond pad opening extending into the insulation layer, the bond pad opening having sidewalls and partially exposing the wiring along the sidewalls;

a conductive layer comprising copper over the substrate and only partially filling the bond pad opening, the layer being on and in contact with the wiring where partially exposed from the insulation layer;

a layer of intermetallic material within the layer comprising copper, the intermetallic material layer comprising copper and palladium, having a thickness of from about 50 to about 150 Angstroms, and defining a bond pad with an outermost surface that is topographically below an outermost surface of the insulation layer immediately surrounding the bond pad opening; and

a conductive connection on the intermetallic layer.

48. (previously presented) The integrated circuit of claim 47 wherein the intermetallic material consists of an intermetallic.

49. (previously presented) The integrated circuit of claim 47 wherein the intermetallic material is less susceptible to formation of metal oxide compared to copper.

50. (previously presented) The integrated circuit of claim 47 wherein the layer comprising copper consists of copper aside from the intermetallic material layer.

51. (previously presented) The integrated circuit of claim 47 wherein the intermetallic material consists of copper and palladium.

52. (cancelled).

53. (previously presented) The integrated circuit of claim 47 wherein about 150 Angstroms of the layer comprising copper is intermetallic material.

54. (original) The integrated circuit of claim 47 wherein the conductive connection comprises an integrated circuit via or an integrated circuit wire bond.

Claims 55-58 (canceled).

59. (previously presented) An integrated circuit comprising:

integrated circuit wiring over a semiconductive substrate;

an insulation layer enclosing the wiring and a bond pad opening extending into the insulation layer, the bond pad opening having sidewalls and partially exposing the wiring along the sidewalls;

a layer consisting of copper over the substrate and only partially filling the bond pad opening, the layer being on and in contact with the wiring where partially exposed from the insulation layer;

a layer of intermetallic material over the copper layer, the intermetallic material layer consisting of copper and palladium, having a thickness of from about 50 to about 150 Angstroms, and defining a bond pad with an outermost surface that is topographically below an outermost surface of the insulation layer immediately surrounding the bond pad opening; and

an integrated circuit wire bond on the intermetallic layer.

60. (previously presented) The integrated circuit of claim 47 wherein the thickness of the intermetallic material layer is sufficient to reduce oxidation of the layer comprising copper.

61. (canceled).

62. (previously presented) The integrated circuit of claim 59 wherein the thickness of the intermetallic material layer is sufficient to reduce oxidation of the layer consisting of copper.